DATA SHEET

BS170
N-channel vertical D-MOS transistor

Product specification
File under Discrete Semiconductors, SC13b

April 1995

Philips
Semiconductors





N-channel vertical D-MOS transistor BS170

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

FEATURES

- Very low $R_{DS(on)}$.
- Direct interface to C-MOS, TTL, etc.
- High-speed switching.
- No secondary breakdown.

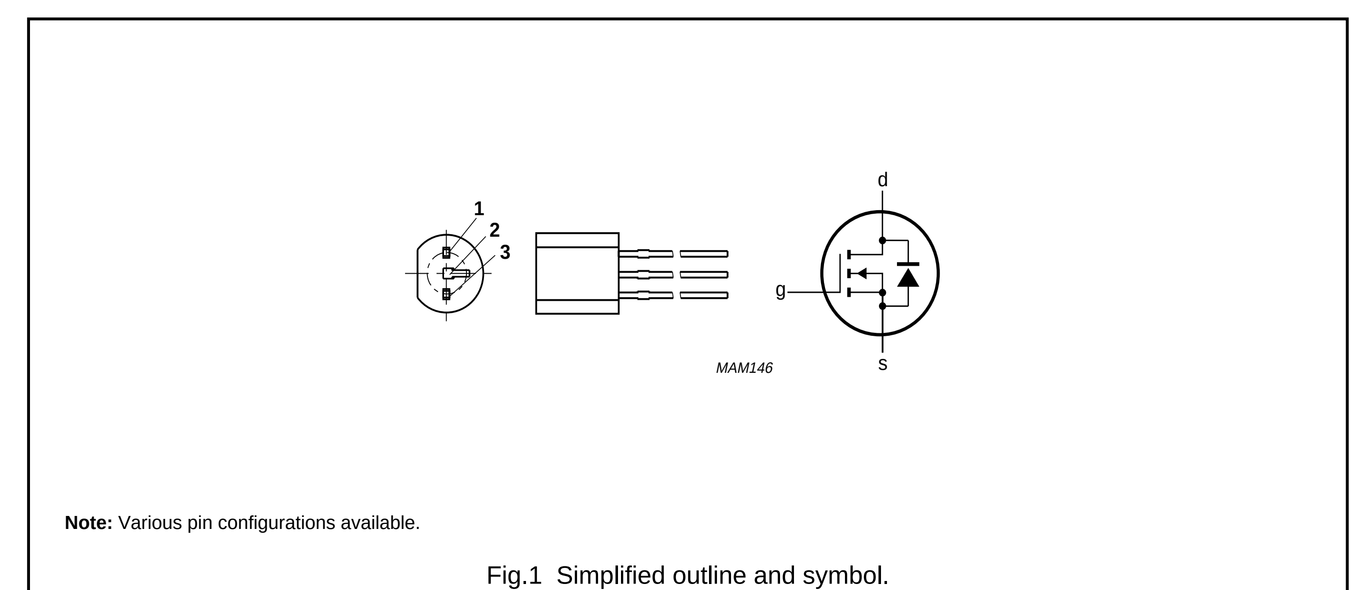
PINNING - TO-92 VARIANT

1 = source
2 = gate
3 = drain

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	60	V
Gate-source voltage	V_{GS}	max.	15	V
Drain current (DC)	I_D	max.	500	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	830	mW
Junction temperature	T_j	max.	150	°C
Drain-source ON-resistance				
V_{GS} = 10 V; I_D = 200 mA	$R_{DS(on)}$	max.	5	Ω

PIN CONFIGURATION



Note: Various pin configurations available.

Fig.1 Simplified outline and symbol.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	60	V
Drain-gate voltage	V_{DG}	max.	60	V
Gate-source voltage	V_{GS}	max.	15	V
Drain current (DC) at T_c = 25 °C	I_D	max.	500	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	830	mW
Storage temperature range	T_{stg}		–55 to +150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	150	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage				
V_{GS} = 0; I_D = 100 μA	$V_{(BR)DS}$	min.	60	V
		typ.	90	V
Gate threshold voltage				
V_{GS} = V_{DS}; I_D = 1 mA	$V_{GS(th)}$	min.	0.8	V
		max.	3.0	V
Gate-source leakage current				
V_{GS} = 15 V; V_{DS} = 0	I_{GSoff}	max.	10	nA
Drain cut-off current				
V_{DS} = 25 V; V_{GS} = 0	I_{DSS}	max.	0.5	μA
Drain-source ON-resistance (note 1)				
V_{GS} = 10 V; I_D = 200 mA	$R_{DS(on)}$	typ.	2.5	Ω
		max.	5.0	Ω
Forward transconductance (note 1)				
V_{DS} = 10 V; I_D = 200 mA; f = 1 kHz	g_{fs}	typ.	200	mS
Capacitances at f = 1 MHz				
V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ.	25	pF
		max.	40	pF
	C_{os}	typ.	22	pF
		max.	30	pF
	C_{rs}	typ.	6	pF
		max.	10	pF
Switching times at I_D = 200 mA				
I_D = 200 mA; V_{DS} = 50 V;	t_{on}	typ.	4	ns
		max.	10	ns
V_{GS} = 0 to 10 V	t_{off}	typ.	4	ns
		max.	10	ns

Note

1. t_p = 80 µs; δ = 0,01.

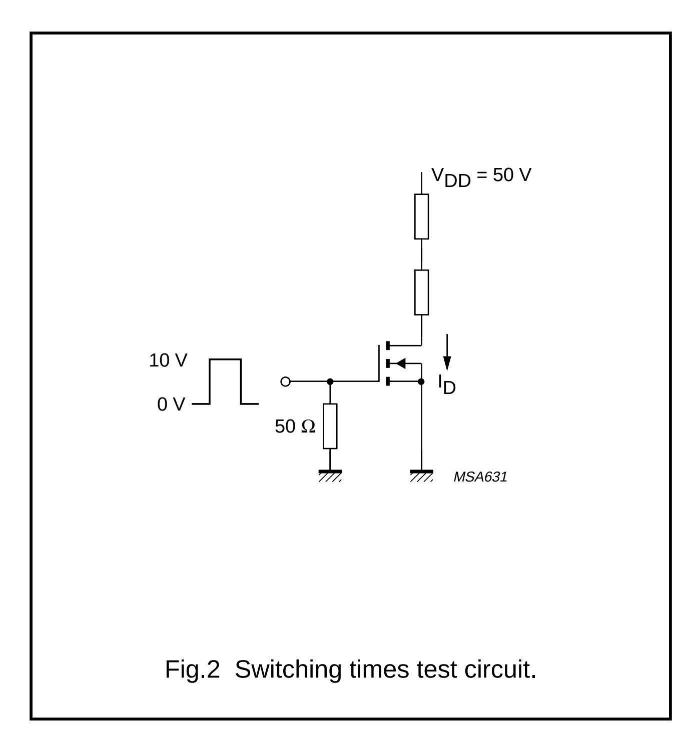


Fig.2 Switching times test circuit.

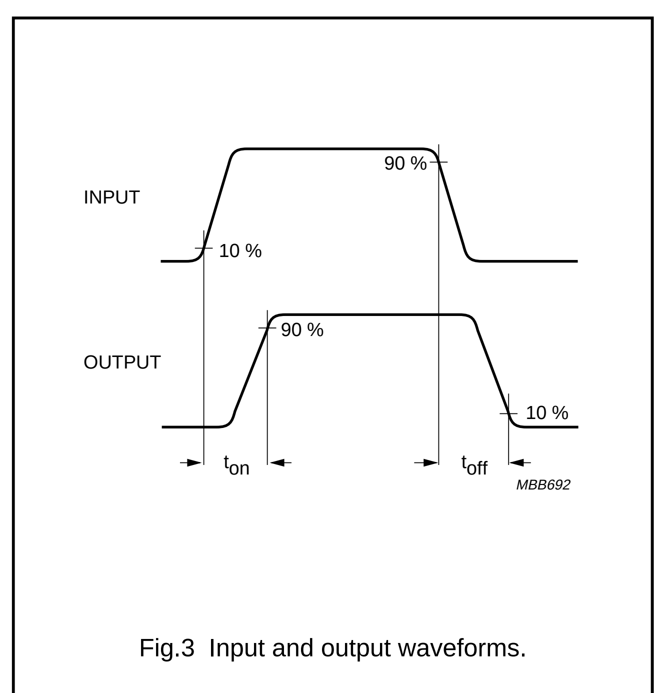
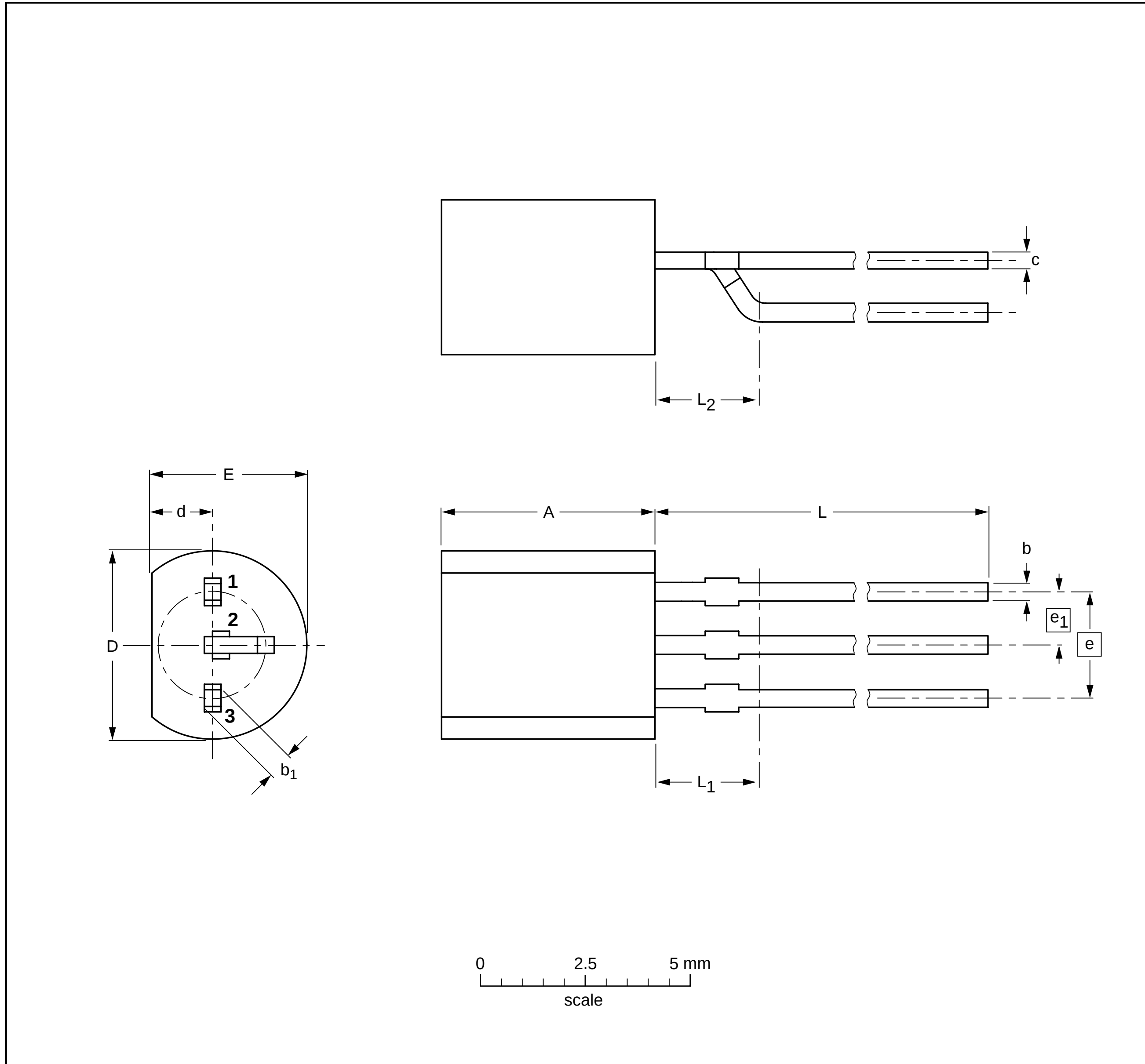


Fig.3 Input and output waveforms.

PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; 3 leads (on-circle) **SOT54 variant**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b_1	c	D	d	E	e	e_1	L	$L_1^{(1)}$ max	L_2 max
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5	2.5

Notes

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT54 variant		TO-92	SC-43			97-04-14

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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Printed in The Netherlands 137107/1200/01/pp8 Date of release: April 1995 Document order number: 9397 750 02456

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